Fast Processor Model of Renesas RL78 CPU Released by Imperas for Open Virtual Platforms

eSOL TRINITY, Imperas Partner, Developed the RL78 Model

OXFORD, United Kingdom and TOKYO, Japan, 31 May 2016 – Imperas™ and eSOL TRINITY announced today the release of the Open Virtual Platforms™ (OVP™) Fast Processor Model for the Renesas RL78 CPU. Example virtual platforms have also been released, as well as support for the new model in the Imperas M*SDK™ advanced software development tools. The model of the RL78 was developed by eSOL TRINITY, Imperas' partner in Japan, providing technical support for Imperas customers as well as services for embedded software development.

The processor core model and example platforms are available from the Open Virtual Platforms website, www.OVPworld.org/Renesas. The model of the RL78 processor core, as well as models of other Renesas processors, work with the Imperas and OVP simulators, including the QuantumLeap™ parallel simulation accelerator, and have shown exceptionally fast performance of hundreds of millions of instructions per second.

"Our customers needed a fast model of the RL78 for software development and testing," said Shuzo Tanaka, Vice President & Director (Tool Development & Sales) of eSOL TRINITY. "We found the OVP technology to be very powerful and easy to use for development of the high performance RL78 processor core model. The Imperas debug and software analysis and test products also provide an excellent software development environment. We are committed to help reduce time and cost for embedded software development with comprehensive solution including Imperas products, technical support, and consultation and engineering services."

All OVP processor models are instruction-accurate, and very fast, part of an embedded software development environment which is available early, so engineers can accelerate the entire product development cycle. Virtual platforms utilizing these OVP processor models can be created with the OVP peripheral and platform models, or the processor models can be integrated into SystemC/TLM-2 based virtual platforms using the native TLM-2 interface available with all OVP processor models.

The OVP models also work with the Imperas advanced tools for multicore software verification, analysis and debug, including key tools for hardware-dependent software development such as OS and CPU-aware tracing (instruction, function, task, event), profiling, code coverage and memory analysis.

"The OVP APIs for model development were made public to allow users to develop, control and own their models and virtual platforms," said Simon Davidmann, president and CEO of Imperas and founding director of the OVP initiative. "It is great to see the OVP model library grow, and the Imperas ecosystem grow, through the development of publicly available models from our partners."

OVP also has the new Extendable Platform Kits™ (EPKs™) from Imperas, which are virtual platforms (simulation models) of the target devices, including the processor model(s) for the target device plus enough peripheral models to boot an operating system or run bare metal applications. The platform and the peripheral models included in the EPKs are open source, so that users can easily add new models to the platform as well as modify the existing models.

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For more information about Imperas, please see www.imperas.com.

About eSOL TRINITY

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